REMARKS

Claims 1-10 are pending in the present application. Claims 1, 4, 5, 9, and 10 have been amended. No new matter has been added.

Claims 1 and 4-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Zhou, et al. (U.S. Patent No. 6,683,481, hereinafter "Zhou"). This rejection is hereby respectfully traversed.

The Examiner specifically remarks that Zhou discloses, "inter alia", a comparator for generating a shortfall signal, an integrator for time integrating the shortfall signal, wherein the output of the integrator is used to generate a reset signal for a microprocessor, and so anticipates the elements of Claim 1.

Applicant respectfully responds that the features recited in Claim 1 prior to the amendments made herein were believed to be patentably distinct over Zhou; however in the interest of advancing the prosecution of this application as expeditiously as possible, Applicant has further amended Claim 1 to recite additional novel features that further distinguish the particular embodiment claimed from the prior art of record. As amended, Claim 1 recites elements not shown, taught or suggested by Zhou.

Claim 1 now recites in part:

> "...a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage, the shortfall signal being a current signal having a value which varies proportionally with the shortfall of the supply voltage in relation to the reference voltage, and

an integrator for time-integrating the shortfall signal to

form an integrated signal..."

Zhou provides a circuit that compares a voltage to a reference level and when the voltage of node DD rises above the reference voltage VREF, the signal BG-PORB goes high (See Col. 9, lines 29-32). That is, Zhou monitors the voltage at node DD and when it is greater than the reference voltage, the output of the comparator goes high. This is in stark contrast to the undervoltage detection circuit of Applicant's claimed embodiment as recited in Claim 1, because Zhou does not report an undervoltage at all; instead Zhou monitors for a healthy supply voltage and outputs a signal only when a situation is detected where there is not an undervoltage.

Further, the reference of Zhou does not disclose integrating a shortfall signal which is generated as a comparator output as recited in Claim 1. Again, in contrast to the Applicant's claimed invention, Zhou has an R-C circuit that receives the double inverse of the comparator output. The device disclosed by Zhou outputs a signal for the charging the capacitor CL only when the supply voltage is in a healthy state; e.g. not an undervoltage. In an undervoltage situation in the circuit of Zhou, no current is flowing through the capacitor CL to be integrated; as the voltage at the node FF is low. Zhou does not show, teach or suggest the integrator required by Applicant's claim recitation.

Accordingly, Applicant believes that Claim 1, and particularly Claim 1 including the amendments made herein, is distinguished over the prior art and is allowable over the rejection. Reconsideration and allowance is therefore requested.

Claim 4 is an independent apparatus claim which incorporates a microprocessor and which recites a shortfall signal and undervoltage detection apparatus very similarly to Claim 1. This claim is also amended herein to further advance the expeditious allowance of the claims and

the application. The amendments to Claim 4 are similar to those for Claim 1 and the arguments made with respect to the Zhou reference again apply to Claim 4. Reconsideration and allowance are therefore respectfully requested.

Claims 5 and 6 were also rejected as anticipated by Zhou. Claim 5 is an independent method claim which recites method steps including steps analogous to the apparatus steps of Claim 1, and the arguments made above with regard to the failing of the Zhou reference to disclose these required elements again apply. Claim 5 recites steps that are not shown, taught or suggested by the Zhou reference, and Applicant concludes that the method of Claim 5 is therefore allowable over the reference and the rejection. Reconsideration is respectfully requested.

Claim 6 depends from Claim 5, adds an additional method step to Claim 5 and necessarily incorporates the allowable method steps from the parent claim. Accordingly, reconsideration and allowance are requested for Claim 6.

Claims 1-2 and 4-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshimura (U.S. Patent No. 5,629,642, hereinafter "Yoshimura") in view of Woods (U.S. Patent No. 6,259,285, hereinafter "Woods"). These rejections are also hereby respectfully traversed.

In his remarks, the Examiner again asserts that it would have been obvious at the time the invention was made to use the delay circuit of Woods in place of the generic delay circuit of Yoshimura, for the purpose of having a delay circuit that is used to delay the output of the comparator 4 to prevent an erroneous RESET signal. The Examiner then asserts that the combination of these references discloses the elements of Claim 1, e.g. a comparator, for generating a shortfall signal, an integrator for time integrating the signal to form an integrated

signal, and where the output of the integrator is used to generate a reset signal. The Examiner also asserts that the combination discloses the discriminator circuit as recited in Claim 2.

Applicant cannot agree with the Examiner's assertions. As argued previously, even in the form the claims had before the present amendments, the claims recited elements distinct from the disclosures of the combination of Yoshimura and Woods. The Examiner asserts that Yoshimura is not limited to the digital circuitry and timing diagrams described in the reference, but the Examiner cannot show a disclosure of the required integrator, instead the Examiner extends the disclosure of the Yoshimura reference, even while admitting the timing diagrams and the description of Yoshimura seems to be describing only digital circuitry, to include analog circuitry and timings not shown in the reference. Thus the obviousness of the rejection seems to be based, not on the disclosure within the reference, but on what the Examiner knows outside of the reference added in combination with the actual disclosure of the reference. This analysis does not meet the required burden of a proper prima facie obviousness rejection, as the cited references do not show or suggest the claimed elements (MPEP 706.02(j)).

In any event, Claim 1 is now further amended and Applicant submits that Claim 1 now particularly recites features not shown, taught or suggested by either Yoshimura, or Woods, and is not obviated by the proposed combination of these references. In particular, Applicant submits that none of the prior art references of record disclose that the output of a comparator (the claimed shortfall signal) is a current signal having a value which varies proportionally with the shortfall of the supply voltage in relation to the reference voltage, as is required by Claim 1. Applicant's claimed embodiment advantageously comprehends both the magnitude of the comparator inputs and the time duration of the shortfall in generating a reset signal, thus the

shortfall signal that is input to the claimed integrator is a function of the comparator input polarity, the magnitude of the comparison, and the time duration of the shortfall.

In contrast, the prior art does not disclose these claimed features. The prior art does not even disclose a need for such features, which is unsurprising as the prior art relied upon is directed to the processing of square wave signals output by their particular digital comparators. Zhou and Yoshimura both disclose digital comparators which output a high or low signal; these signals are supplied to digital inverters. Neither of the primary references, nor the Yoshimura reference in combination with Woods, shows, teaches or suggests the variable current signal as claimed.

Accordingly Applicant believes that Claim 1 is allowable over the rejection. Reconsideration and allowance are respectfully requested for Claim 1.

Claim 2 depends from and adds elements to the allowable features of Claim 1, and is therefore also believed to be allowable. Reconsideration and allowance is therefore respectfully requested.

Claim 4 is an independent apparatus claim which recites a microprocessor, along with circuitry similar to that recited in Claim 1, and is therefore also believed to be allowable. Claims 5 and 6 are method claims which recite (Claim 5) method steps that are analogous to the apparatus elements of Claim 1 and which are also believed to be unobvious over the references and allowable over the combination and the rejection. Claim 6 is a dependent claim which adds a method step to the method of Claim 5, and necessarily incorporates the allowable method steps of Claim 5 and is therefore also believed to be allowable. Reconsideration and allowance are therefore respectfully requested for each of Claims 4-6 over the rejections.

Applicant acknowledges the finding of allowability over the prior art of record for Claims 9 and 10. With respect to the claims objected to, Applicant acknowledges the Examiners findings that Claims 3 and 8 would be allowable if rewritten in an independent form, however in light of the amendments and arguments made herein, each of these claims is now believed to depend from and recite additional elements or steps on an allowable independent parent claim, and therefore to be allowable without further amendment. Reconsideration and withdrawal of the objections to Claims 3 and 8 is respectfully requested.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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